BLF888E; BLF888ES

UHF power LDMOS transistor

AMPLEON

Rev. 1 — 17 March 2016 Objective data sheet

1. Product profile

1.1 General description

A 750 W LDMOS RF power transistor for broadcast Doherty transmitter applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications.

Table 1. Application information

RF performance at V_{DS} = 50 V in an asymmetrical Doherty application.

Test signal	f	$P_{L(AV)}$	G_p	η_D	IMD_{shldr}	PAR
	(MHz)	(W)	(dB)	(%)	(dBc)	(dB)
DVB-T (8k OFDM)	470 to 590	150	17	52	−38	8 [1]
	580 to 690	<tbd>	<tbd>	<tbd>	<tbd>	<tbd>
	650 to 790	150	15	49	−38	8 [1]

[1] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

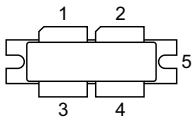
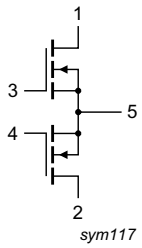
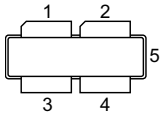
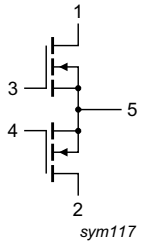
- Designed for asymmetric Doherty operation
- High efficiency
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Broadcast transmitter applications in the UHF band
- Digital broadcasting

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF888E (SOT539A)			
1	drain1 (peak)		
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source [1]		
BLF888ES (SOT539B)			
1	drain1 (peak)		
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF888E	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF888ES	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS(amp)main}$	main amplifier drain-source voltage		-	104	V
$V_{DS(amp)peak}$	peak amplifier drain-source voltage		-	120	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		−0.5	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		−6	+11	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 150 W [1]	<tbd>	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.4 mA	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 240 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	38	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 8.5 A	-	120	-	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.6 mA	120	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 360 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	57	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 12.6 A	-	90	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	210	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	67	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	1.35	-	pF
Peak device						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	315	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	105	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	1.5	-	pF

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Table 8. RF characteristics

RF characteristics in Ampleon production test circuit, T_{case} = 25 °C; unless otherwise specified.

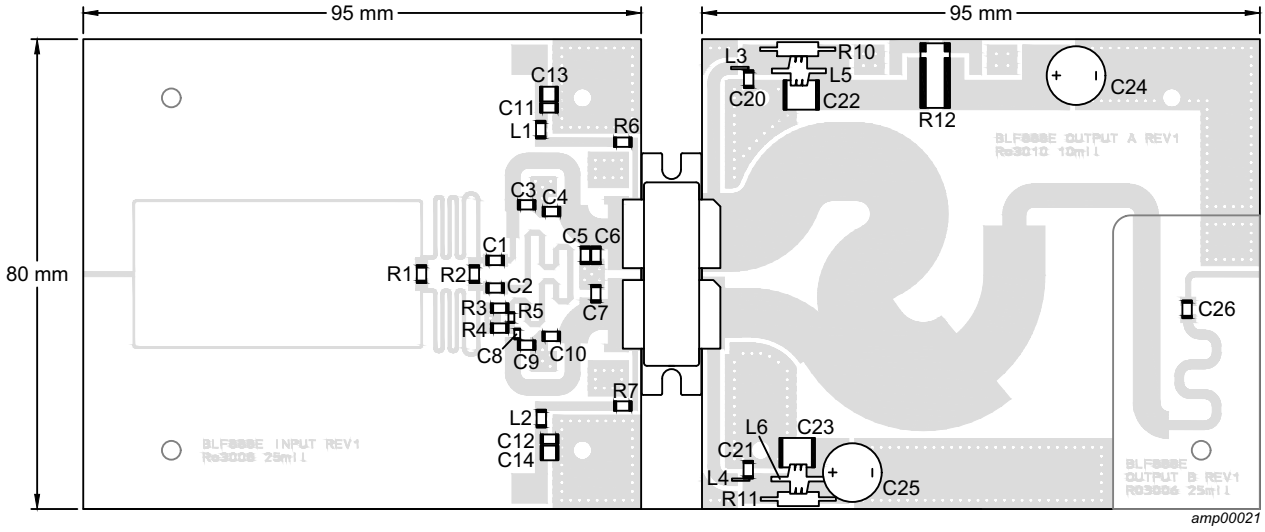
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVB-T (8k OFDM), class-AB						
V_{DS}	drain-source voltage		-	50	-	V
I_{Dq}	quiescent drain current	peak section: V_{GS} = 1.3 V below $V_{GS(th)}$ (peak)	-	600	-	mA
$P_{L(AV)}$	average output power	f = 550 MHz	-	150	-	W
G_p	power gain	f = 550 MHz	15.3	17	-	dB
η_D	drain efficiency	f = 550 MHz	47	52	-	%
IMD_{shldr}	intermodulation distortion shoulder	f = 550 MHz	-	−24	−21	dBc
PAR	peak-to-average ratio	f = 550 MHz	-	7.8	-	dB

7. Test information

7.1 Ruggedness in Doherty operation

The BLF888E and BLF888ES are capable of withstanding a load mismatch corresponding to VSWR ≥ <tbd> through all phases under the following conditions: V_{DS} = <tbd> V; f = <tbd> MHz at rated load power.

7.2 Test circuit



Printed-Circuit Board (PCB): Rogers 3006; ε_r = 6.5 F/m; height = 0.635 mm; Cu (top/bottom metalization); thickness copper plating = 29.6 μm; Rogers 3010: ε_r = 10 F/m; height = 0.254 mm

See Table 9 for a list of components.

Fig 1. Component layout for production RF test circuit

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Table 9. List of components

For test circuit see Figure 1.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	51 pF [1]	ATC 100B
C3	multilayer ceramic chip capacitor	11 pF [1]	ATC 100B
C4	multilayer ceramic chip capacitor	13 pF [1]	ATC 100B
C5, C6	multilayer ceramic chip capacitor	24 pF [1]	ATC 100B
C7	multilayer ceramic chip capacitor	33 pF [1]	ATC 100B
C8	multilayer ceramic chip capacitor	51 pF [2]	ATC 100A
C9	multilayer ceramic chip capacitor	12 pF [1]	ATC 100B
C10	multilayer ceramic chip capacitor	20 pF [1]	ATC 100B
C11, C12	multilayer ceramic chip capacitor	43 pF [1]	ATC 100B
C13, C14	multilayer ceramic chip capacitor	4.7 μF	
C20, C21	electrolytic capacitor	100 pF [1]	ATC 100B
C22, C23	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C25, C25	electrolytic capacitor	470 μF, 63 V	
C26	multilayer ceramic chip capacitor	47 pF [1]	ATC 100B
L1, L2	inductor	10 nH	Coilcraft
L3, L4	inductor	0.5 turn, D = 2 mm, d = 1mm	
L5, L6	inductor	1 turn, D = 5 mm, d = 1mm	
R1	chip resistor	90 Ω	
R2	chip resistor	265 Ω	
R3, R4	chip resistor	360 Ω	
R5	chip resistor	15 Ω	
R6	chip resistor	75 Ω	
R7	chip resistor	5 Ω	
R10, R11	wire resistor	1 Ω	
R12	shunt resistor	0.01 Ω	

[1] American Technical Ceramics type 100B or capacitor of same quality

[2] American Technical Ceramics type 100A or capacitor of same quality

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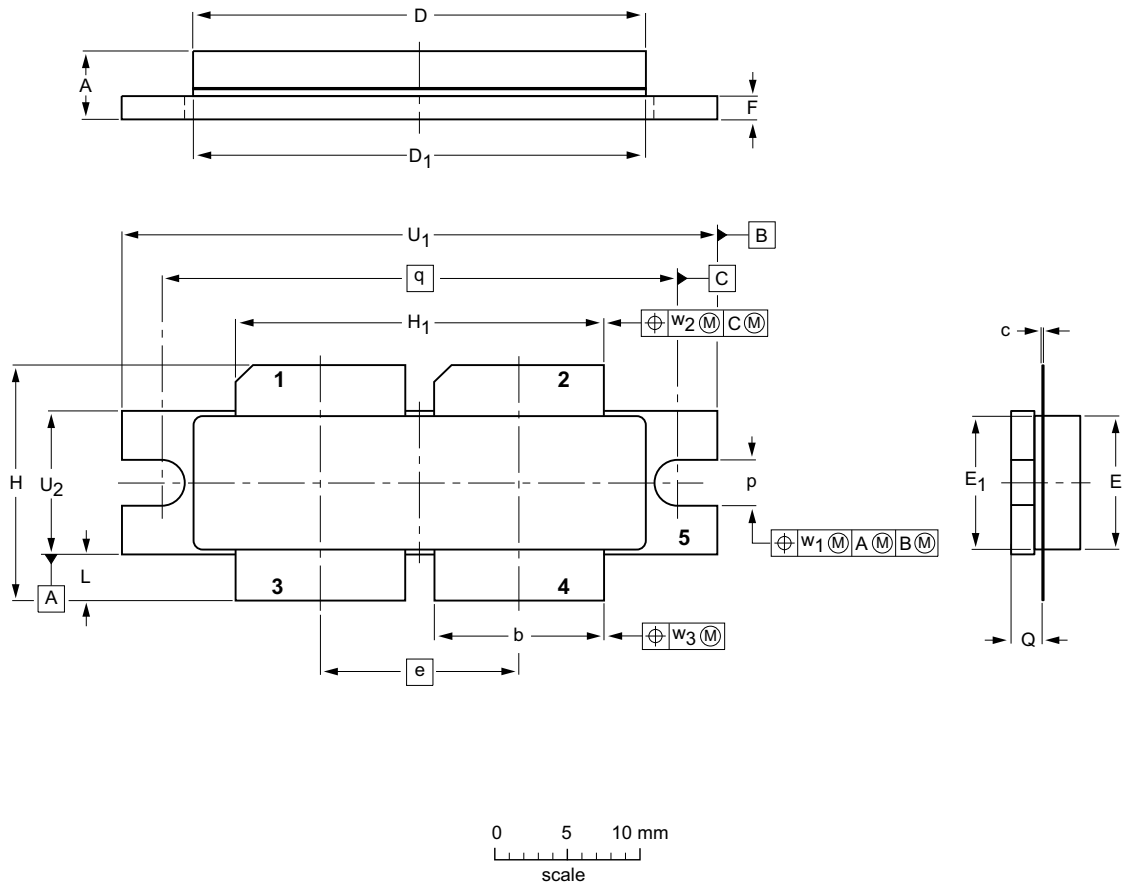
8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 2. Package outline SOT539A

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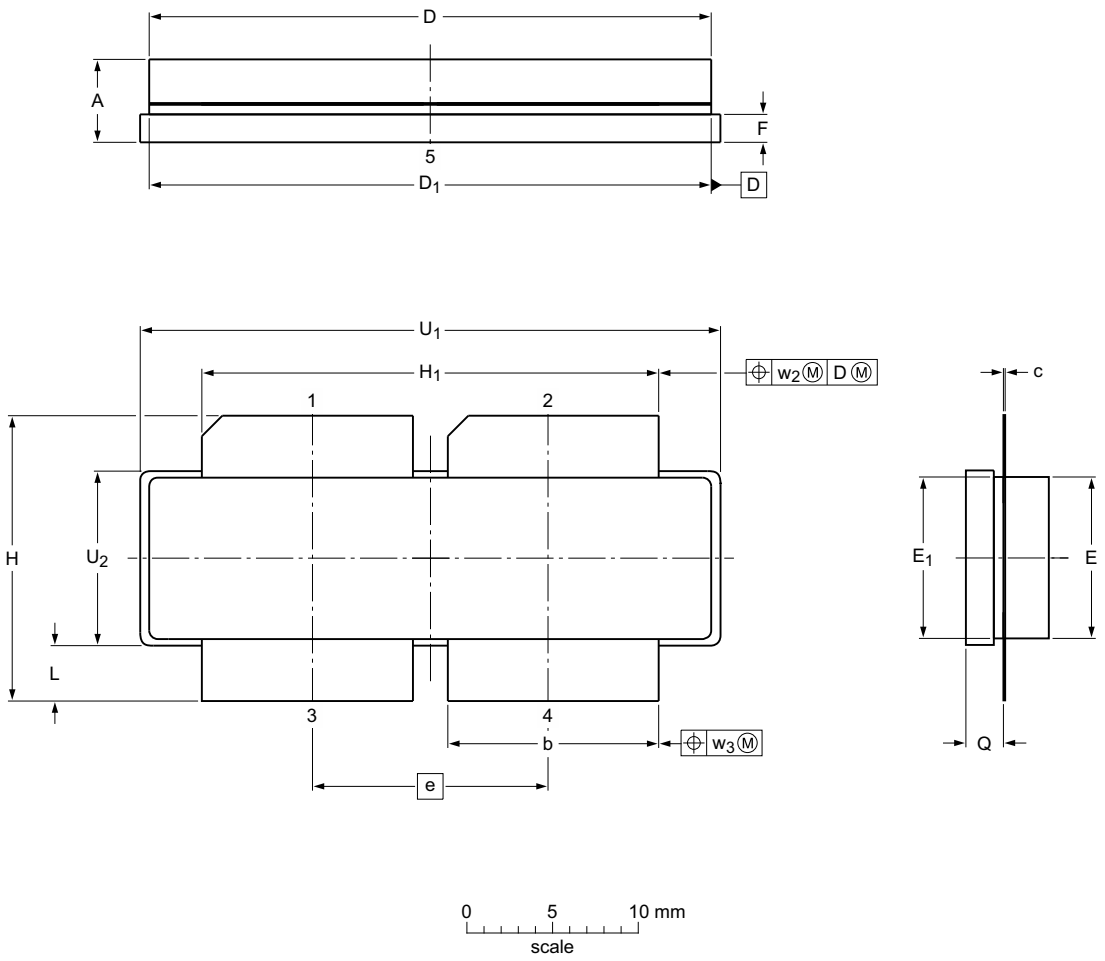
Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 3. Package outline SOT539B

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9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
UHF	Ultra High Frequency

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF888E_BLF888ES v.1	20160317	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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